Accurate, Wideband Characterization and Optimization of High Power LDMOS Amplifier Memory Properties

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Abstract - **Accurate, wideband measurements of high power LDMOS PCS band stages were carried out in an effort to quantify their memory characteristics. The measurements help identify intrinsic and extrinsic sources of memory in addition to a measurable parameter that can be used for improved design. Results of successful circuit optimization for memory are also presented.**

I. INTRODUCTION

So-called memory effects in high power RF amplifiers have been a subject of intensifying investigations lately [1]-[2]. This is a rather new category of distortion that has caught the attention of power amplifier designers, although the phenomenon and its implications are quite well known in communication systems in general [3]-[5]. Not only the physical origins of memory effects are various and vague, it is also difficult to model and analyze this phenomena by the traditional tools and methods that are currently familiar to power amplifier designers. It has become necessary to understand and manage this effect as non-traditional, digital modulation schemes have become more popular, bringing about the need for linearized transmitters. It has been found that without a good understanding and control, if not total elimination, of memory from all related circuits, it is difficult to realize the full potential of various linearization methods. Some types of linearization, such as predistortion are especially sensitive to memory effects.

We will describe here work done to better measure and quantify memory experimentally and also understand basic characteristics and implications for linear PA design. We will describe a high performance two-tone characterization system and show test results on some high-power LDMOS devices commonly used in the output design of PAs.

II. MEMORY

Memory effects have mostly come to the attention of PA designers through observed asymmetry in the output IM products of certain amplifier designs [6]-[7]. It was also noticed that the amount of asymmetry was affected by bias terminations. It is also known that thermal time constants can also result in memory behavior and it is quite possible to observe all this phenomena in time domain [8]-[9]. It can be shown analytically that since in reality the IMD products observed are usually a vector combination of various orders, the variations and asymmetry can be explained to a large degree by exposing the relative phase variations between these components as a function of frequency, terminations and drive. More specifically, for a simple 3rd order nonlinearity, it can be shown that [3]-[6]:

$$IM3_U = \left[H_2(\omega_2-\omega_1)\cdot H_1(\omega_2)+H_2(2\omega_2)\cdot H_1(-\omega_1)+H_3(2\omega_2-\omega_1)\right]e^{j(2\omega_2-\omega_1)}$$

$$IM3_L = \left[H_2^*(\omega_2-\omega_1)\cdot H_1(\omega_1)+H_2(2\omega_1)\cdot H_1(-\omega_2)+H_3(2\omega_1-\omega_2)\right]e^{j(2\omega_1-\omega_2)}$$

Where $H_n(\omega)$ is the nth order frequency domain Volterra kernel. What is missing from most of these demonstrations is a reasonable measure of this quantity, asymmetry, which we associate with memory, and relating it to the basic design parameters available to a PA designer.

III. SET UP AND TEST DEVICES

We have assembled a 2 GHz two-tone set up (Fig. 1) using two separate clean sources, driving separate linear PAs. The individual IM tones are accurately measured with a pair of synchronized network analyzers serving as very sensitive calibrated receivers. A high-speed digital oscilloscope is used for base-band analysis at various points of the test circuit. All instruments are on a control bus and all calibration, data collection and performance verification is done electronically. This arrangement allows for very accurate two-tone sweeps of both frequency and power. All extraneous time constants have been eliminated in addition to thermal distortions and internally generated IM products. Power asymmetry between the pair of tones is better than 0.1 dB under all conditions. The system is also reconfigurable to make digital and time domain measurements, which will not be presented here.

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The devices of interest were 2.1 GHz, 120 W and 180 W, push-pull Motorola LDMOS parts, commonly used in PA designs in this band. A typical test circuit was built using traditional design methods without particular attention to memory performance. The circuit was optimized for wide-band power and IMD performance with flat gain. In addition to CW characterization to confirm proper and optimum operation of the single-stage modules, swept measurements were carried out with two tones for frequency separation up to 30 MHz, and with varying bias and drive conditions. Difference in lower and upper side 3rd and 5th order IMDs, which were taken as a measure of memory, were plotted. The 120 W module was measured as a baseline and the 180 W module was measured and also optimized for memory.

IV. RESULTS AND ANALYSIS

In Fig. 2, lower and upper 3rd and 5th order IMDs are shown vs. frequency spacing with input power as a parameter. Input power of 27dBm/tone corresponds to Pout of 43 dBm for two tones, which is the nominal Pout for this 120 W device as a W-CDMA PA stage. Fig.3 shows the difference between upper and lower IMDs vs. frequency spacing for the 3rd order IMD with Pin as a parameter. Note the sign change. Fig. 4 shows the same data but with constant nominal Pin at 27 dBm and bias current as a parameter. Not only there are strong resonances in the response but they also move with bias.

For the 120 W push-pull stage (that was designed without memory considerations), the maximum difference between upper and lower 3rd order IMDs as a function of frequency spacing and with constant input power of 27 dBm/tone, was about 12 dB. When the input power was reduced by 1 dB, the maximum difference was as high as 30 dB, where the worst case was at small frequency spacing (see Fig.3). This is found to be typical when large series resistors are used in the gate bias circuit.

Fig. 4 data is also very significant which indicates the strong dependence of memory to the operating point, which is also related to the drive level obviously since these are AB-biased stages. Note that for 120 W device, the optimum IMD performance also corresponds to the worst memory behavior (for this particular circuit realization). This would be detrimental for a predistortion linearization of this stage. Drastic variation of the memory asymmetry with slight change in the operating point for the same port impedances clearly points out to the potentially substantial intrinsic device contribution to the memory effect.

For 180 W device, after optimization for memory, the maximum difference between upper and lower 3rd order IMDs as a function of frequency spacing, and with constant (nominal) input power of 29 dBm/tone, was about 3 dB (Fig. 5). Asymmetry was almost 20 dB at 10 MHz before the optimization. Response above 20 MHz was not effected by the tuning..

The strong variation of 3rd order IMDs for frequency spacing grater than 20MHz, seem to be related to the 1st and 2nd sub-harmonics, see Fig. 6. Push-pull topology and bias networks themselves make absolute power level comparisons difficult.

The general approach to optimization was to minimize the 2nd harmonic and the 1st and the 2nd sub harmonics while maintaining acceptable P_{1dB} level and power efficiency. Each such tuning was done independently while monitoring in real time the second harmonic, the sub harmonic (1st and 2nd) and the 3rd order IMDs. As results indicate, it is possible to optimize the wideband memory characteristics of a PA circuit with some reasonable compromise in RF performance.

V. CONCLUSION

Memory effects are manifested in a circuit when odd and even order distortion components interact with each other, through the feedback and complex port impedances, which are functions of frequency separation, operating point and drive. There are both circuit, and intrinsic device contributions to the memory behavior. This is one reason why it may not be possible to eliminate memory completely by circuit optimization for certain device designs and technologies.

Even though IMD asymmetry is a good measure of memory, by itself does not capture the whole picture as any baseband response other than unity indicates presence of memory. Two-tone measurements in frequency domain are a good way to probe the envelope response of the circuit in question, though for a complete picture it would be desirable to carry out such characterizations in modulation or envelope domain. This would also allow for development of a baseband memory compensation method. Still, for practical reasons, and especially for DPD applications, real wide-band envelope response, or memory, needs to be optimized at the circuit level.

As shown here, it is possible to optimize the envelope response or memory characteristics of a PA stage through circuit and operating point improvements, but since in practice the number of frequency components and modulation formats, ports and other important RF parameters to be traded off is a rather large set, a method of multi-port and multi-tone load-pull optimization would be very desirable for best results [10].

REFERENCES

[1] Steve C. Cripps, Advanced Techniques in RF Power Amplifier Design, Artech House, Boston, 2002.

[2] Wolfgang Boesch, Giuliano Gatti, "Measurement of Memory Effects in Predistortion Linearizers", IEEE MTT-S Digest, 1989.

[3] Stephen A. Mass, Nonlinear Microwave Circuits, Artech House, 1998.

[4] M. Schetzen, "The Volterra and Weiner Theory of Nonlinear Systems", John Wiley and Sons, 1980.

[5] J. F. Barrett, " The Use of Functionals in the Analysis of Nonlinear Physical Systems," *Journal of Electronics and Control*, Vol. 15(6), pp. 567–615, 1963.

[6] J. F. Sevic, K. L. Burger ,"A novel envelope-termination load-pull method for ACPR optimization of RF/Microwave power amplifiers", 1998 IEEE MTT-S Digest, pp 723-726.

[7] Joel H. K. Vuolevi, Timo Rahkonen, Jani P. A. Manninen, Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers, IEEE Trans. MTT, Vol 49, No. 8, August 2001.

[8] N. Le Gallou, J.M. Nebus, E. Ngoya , H. Buret, "Analysis Of Low Frequency Memory And Influence On Solid State HPA Intermodulation Characteristics", 2001 IEEE MTT-S Intl. Microwave Symp, May 2001.

[9] C.J. Clark, G. Chrisikos, & Al., "Time-Domain Envelope Measurement Technique with Application to Wideband Power Amplifier Modeling", IEEE Trans. MTT., vol. 46, no. 12 December 1998, pp25

[10] Fadhel M. Ghannouchi, Robert Larose, Renaro G. Bosisio, "A New Multiharmonic Loading Method for Large-Signal Microwave and Milimeter-Wave Transistor Characterization", IEEE Trans. MTT, Vol 39, No. 6, June 1991.

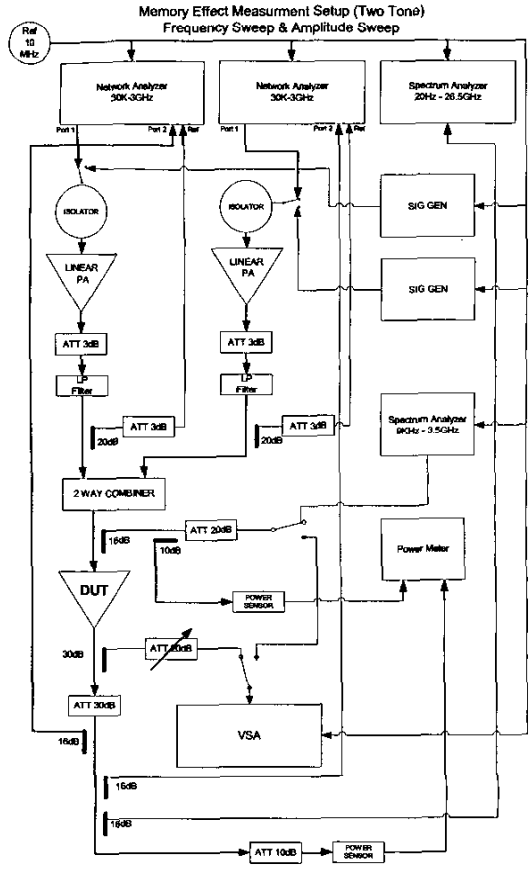

Fig. 1 – Memory characterization system

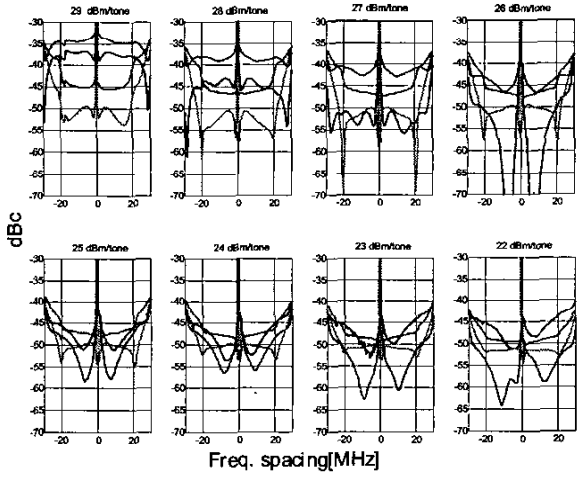

Fig. 2 – 3rd and 5th order IMDs as a function of tone spacing and drive level. (Red-upper 3rd, Blue-lower 3rd, Dark Grn-upper 5th, Light Grn-lower 5th)

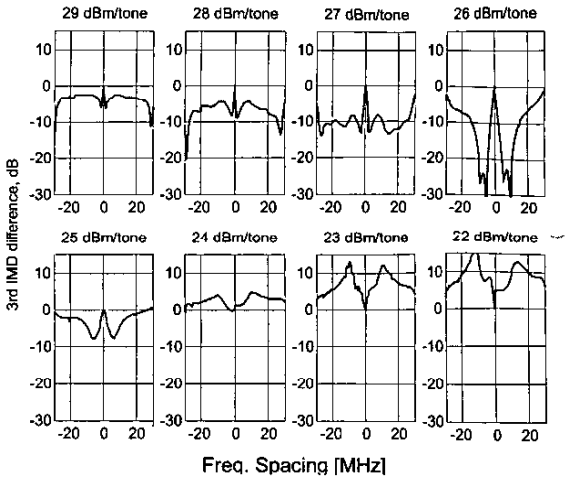

Fig. 3 – IMD asymmetry plotted as a function of Pin. Nominal level is 27 dBm/tone.

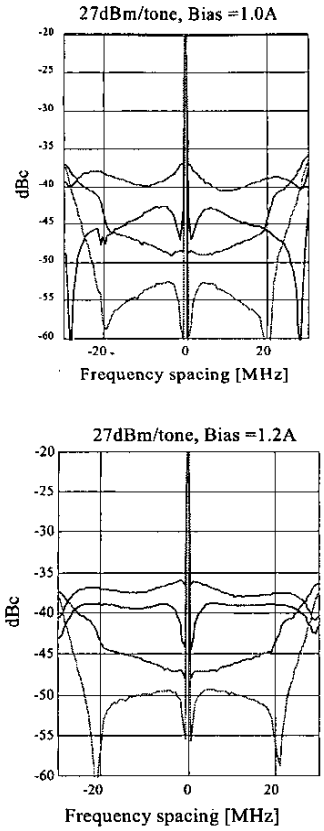

Fig. 4 – 3rd and 5th order IMDs as a function of operating point (red/blue 3rds).

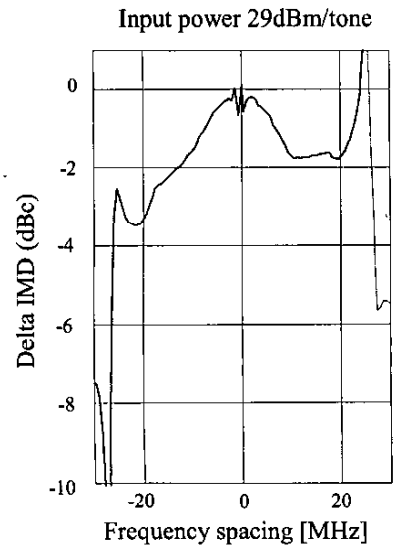

Fig. 5 – Asymmetry of the 180 W stage after circuit optimization for memory.

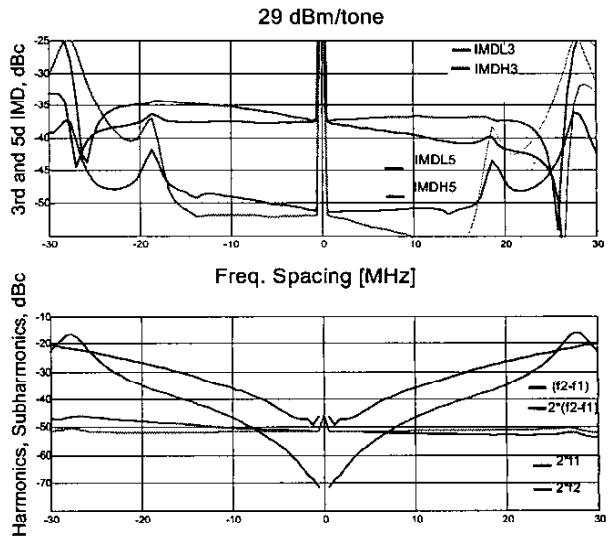

Fig. 6 – Plot of distortion terms, sub-harmonics and harmonics as function of tone separation.